

Docket No.: 60188-538

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Hideo OISHI

Serial No.: Divisional of Appln.

Serial No. 09/905,922

Group Art Unit: Not yet assigned

Filed: June 25, 2003

Examiner: Not yet assigned

For: SEMICONDUCTOR WAFER TEST SYSTEM

INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached form PTO-1449. It is respectfully requested that the references be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

The references were cited by or submitted to the U.S. Patent and Trademark Office in parent application Serial No. 09/905,922, filed July 17, 2001, which is relied upon for an earlier filing date under 35 USC 120. Thus, copies of these references are not attached. 37 CFR 1.98(d).

Respectfully submitted,

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